08-31-04

2811

Atty. Dkt. No. 039153-0688

IFW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ihsan J. DJOMEHRI

Title: STRAINED SILICON MOSFETS HAVING NMOS GATES WITH WORK FUNCTIONS FOR COMPENSATING NMOS THRESHOLD VOLTAGE SHIFT

Appl. No.: 10/738,496

Filing Date: 12/17/2003

Examiner: V. Hung

Art Unit: 2811

CERTIFICATE OF EXPRESS MAILING

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August 30, 2004 (Date of Deposit)

Ruthie Vallejo (Printed Name)

(Signature)

RESPONSE TO RESTRICTION REQUIREMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the restriction requirement set forth in the Office Action mailed August 13, 2004, Applicant hereby provisionally elects Group II, Claims 9-22, drawn to a method of making a semiconductor device, classified in class 438, subclass 592. Applicant reserves the right to file a divisional application on the non-elected claims.

Respectfully submitted,

Date 30 August 04

By Ronald Coslick

FOLEY & LARDNER LLP
Customer Number: 23392
Telephone: (310) 975-7964
Facsimile: (310) 557-8475

Ronald Coslick
Attorney for Applicant
Registration No. 36,489